A K/Ka-Band Distributed Power Amplifier with Capacitive Drain Coupling

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A 14 to 37 GHz MMIC distributed power amplifier has been demonstrated. The amplifier has three FETs of varying periphery, all capacitively coupled to the gate line. A new circuit concept has been used to increase output power, the drain of the last FET is capacitively coupled to the drain line. 4 dB gain has been achieved from 14 to 37 GHz. Output power of 20 dBm or greater has been demonstrated at frequencies up to 33 GHz at 1 dB compression. A maximum 1 dB compressed output power of 23.5 dBm (220mw) has been measured at 26 GHz. The circuit is truly monolithic, with all bias and matching circuitry included on the chip.

INTRODUCTION

Distributed amplifiers have been demonstrated operating up to Ka band with output power levels of 12 to 15 dBm [1][2]. Varying FET size can be utilized to increase total FET periphery, resulting in higher gain and somewhat higher output power [1]. At lower frequencies it has been demonstrated that capacitively coupling FET gates to the gate line allows total FET periphery to be increased dramatically, resulting higher output power without a significant change in gain [3].

This work was supported in part by the U.S. Army, LABCOM/EDTL, Fort Monmouth, NJ, under contract no. DAAL01-86-C-0018.

The gate coupling capacitors allow total FET periphery to be increased by reducing gate loading on the gate line.

As total FET periphery is increased by the use of gate coupling capacitors, drain line loading begins to limit output power, particularly at the upper end of the operating band. The resulting output power cut-off is lower in frequency than the small signal gain cut-off.

Insight into the effects of the drain line loading may be gained by calculating the impedance at the drain nodes of the FETs. This impedance is calculated as the ratio of the voltage at the node to the current through the node, with all FETs connected and active. When drain line loading occurs, the real part of the impedance at the drains of the FETs nearest the output becomes very low and sometimes negative at the upper end of the operating band. When the real part of the impedance is low, the FET contributes very little to the total output power. When the real part of the impedance is negative, the FET is absorbing more rf power than it generates. This is the power limiting mechanism.

Once drain line loading begins to limit output power, higher output power cannot be achieved by changing periphery. Further increasing the total FET periphery increases the output current capacity of

the FETs, but since it also causes drain impedance to decrease, and total output power does not increase. Drain line loading may be avoided by reducing periphery, but FET output current capacity is also reduced, and total output power does not improve.

A new technique has been devised to increase output power. A capacitor is inserted between the drain line and the drain of any FET seeing a low or negative impedance. This deceases drain line loading and increases the impedance at the drains. High total FET periphery can be accommodated, thus higher output power may be achieved.

CIRCUIT EXAMPLE

An example of a distributed amplifier using capacitive drain coupling is shown in Figure 1. This circuit, operating from 14 to 37 GHz, also features varying gate periphery and capacitive gate coupling. Total FET periphery is 1.03 mm. A drain coupling capacitor is used at FET3. Without this capacitor, power is limited by low impedance at the drains of FET3 and FET2. Simulation shows that adding this capacitor increases power by 1 to 3 dB at frequencies above 20 GHz.

Normally the drains of all FETs are biased through the drain line. The addition of the drain coupling capacitor

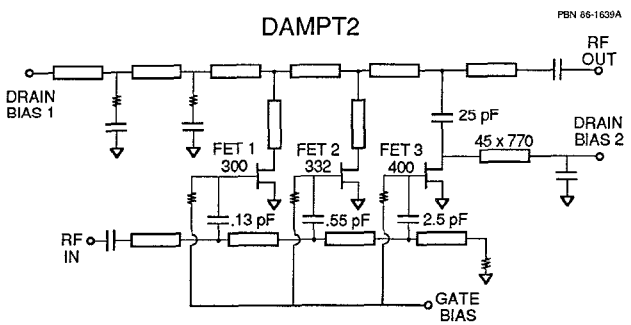

Figure 1. Circuit Schematic

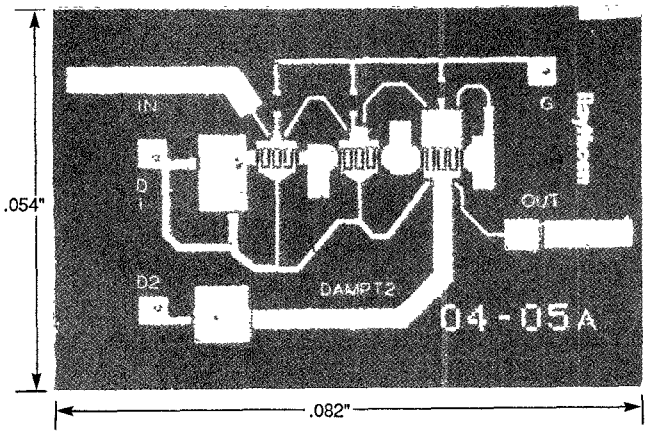

Figure 2. Photo of Amplifier MMIC

prevents FET3 from being biased this way. Instead, a separate drain bias network is used for FET3, comprised of a large capacitor and a quarter-wave transformer. It is important that the bias network present a very high impedance in order to avoid degrading amplifier performance. A quarter-wave transformer presents a sufficiently high impedance over frequency bands of an octave or greater.

CIRCUIT PERFORMANCE

The completed circuit is shown in Figure 2. The circuit is fully monolithic, all bias circuitry is included on the chip. MBE material was used with an active layer carrier concentration of 4.5×10^{17} cm^{-3} and a contact layer concentration of 3×10^{17} cm^{-3}. The FETs have 0.25 micron gates. Silicon Nitride with a thickness of 0.2 microns was used both as a capacitor dielectric and as passivation. The complete chip measures 54 x 82 mils (1.4 x 2.1 mm). The dc I-V curves of all the FETs in the amplifier in parallel (1.03 mm total periphery) are shown in Figure 3.

The measured small signal performance of the amplifier is shown in Figure 4. Flat 4-5 dB gain has been achieved from 14 to 37 GHz with the FETs biased at I_{dss}.

Input return loss is better than 10 dB at the bottom of the band, but gradually degrades to 6 dB at the top of the band. Output return loss is better than 10 dB except at the bottom of the band where it is 8 dB.

Power performance was measured under the same bias conditions as small signal performance (I_{dss}), and is summarized in Figures 5. Figure 5 shows output power curves at various input power levels, as well as 1 dB and 1.5 dB compression curves.

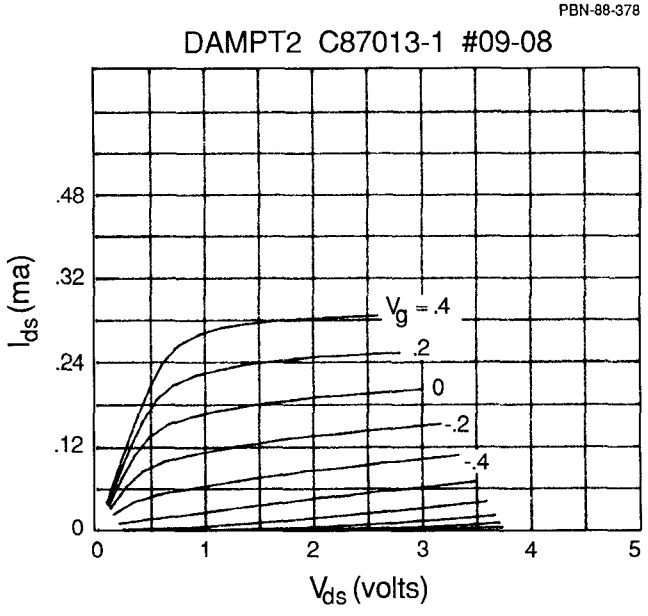

Figure 3. Amplifier DC I-V Characteristics (Chip 1).

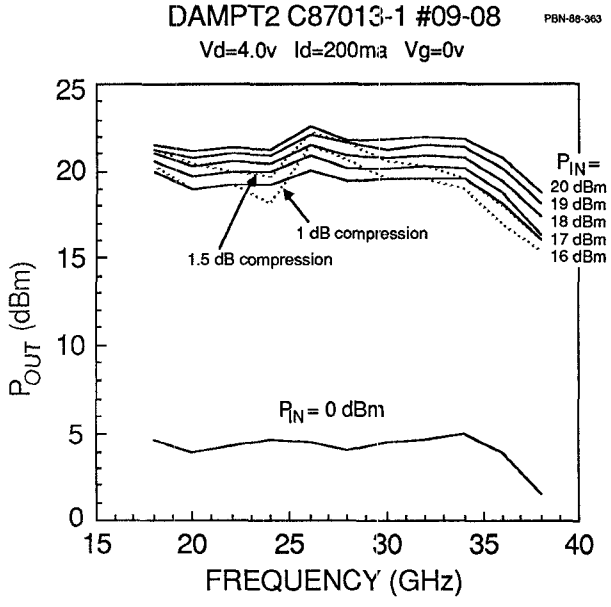

Figure 5. Measured Amplifier Power Performance (Chip 1).

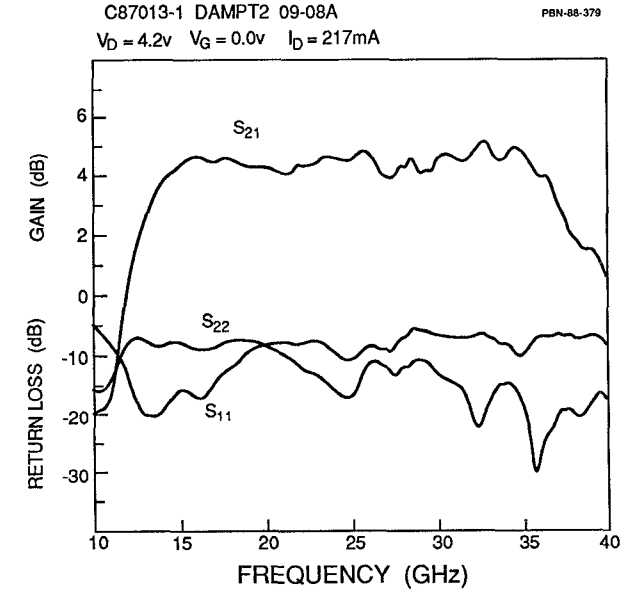

Figure 4. Measured Amplifier Small Signal Performance (Chip 1).

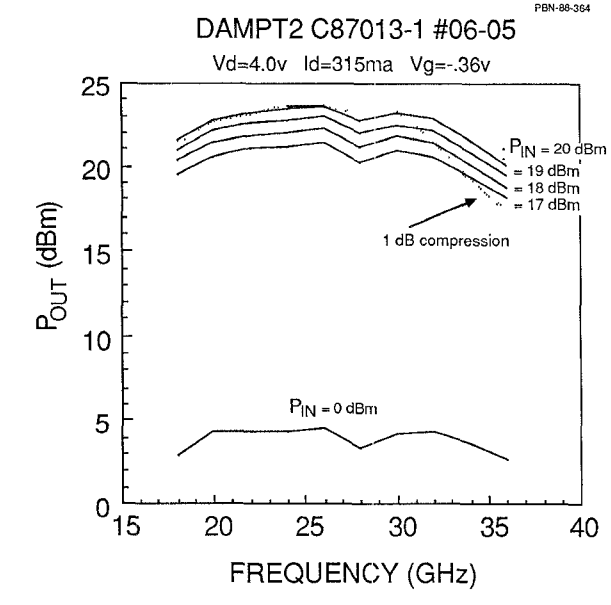

Figure 6. Measured Amplifier Power Performance (Chip 2).

A curve at 0 dBm input power is included for convenient verification of small signal performance. At 1 dB compression, output power is better than 19 dBm up to 34 GHz. At 1.5 dB compression output power is better than 20 dBm up to 34 GHz, and better than 19 dBm to 35 GHz.

The power performance of an additional chip is shown in Figures 6. This chip has FETs with higher I_{dss} and slightly lower gain. Better than 20 dBm has been achieved to 33 GHz at 1 dB compression. A maximum 1 dB compressed power of 23.5 dBm (220 mw) has been achieved at 26 GHz. The small signal gain of this chip is indicated by the P_{in}=0 dBm curve at the bottom of Figure 6.

SUMMARY

A K/Ka-Band distributed power amplifier has been demonstrated in MMIC form. It incorporates a novel circuit feature, capacitive drain coupling. The drain coupling capacitor reduces drain line loading, increasing the impedance seen by the FET, and results in higher output power. More than 100 mw has been achieved up to 34 GHz.

ACKNOWLEDGEMENT

The authors would like to thank R. Binder for measurements, A. Platzker and J. Cole for assistance in distributed amplifier power analysis, H. Renaud and P. Hatch for layout, M. Weiler for assistance with device modelling, E. Tong for assistance in device development and W. Hoke for MBE material

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